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Multilevel Beam SOI-MEMS for Optical Applications

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***Abstract* – A microfabrication technology has been developed and demonstrated, which enhances the capabilities and applications of high aspect ratio silicon-on-insulator microelectromechanical systems (SOI-MEMS) by enabling additional independent degrees of freedom of operation: both upward and downward vertical pistoning motion as well as bi-directional rotation. This is accomplished by applying multiple-mask high aspect ratio etches from both the front- and back-side of the SOI device layer, forming beams at different levels. The processes utilize four masks, two for front-side and two for back-side etching. As a result, single-crystal silicon beams with four different cross-sections are fabricated, and can be combined to form many additional beam cross-sections. By this methodology, unique high aspect ratio micromirror devices were demonstrated with fully isolated and accurately self-aligned vertical combdrives in the SOI device layer, with initial combfinger overlap. Examples of fabricated devices are given.**

I. INTRODUCTION

The recent focus of the MEMS world on optical applications of micromachined devices has pushed the field out of surface micromachining technology [1]-[4]. This is mainly due to the need for optically very flat and smooth structures, as well as due to the desire for large deflections and large actuation forces available using high aspect-ratio micromachining. Silicon on insulator (SOI) based MEMS have become increasingly interesting recently as a platform for a variety of optical applications [5]-[10]. By moving to silicon on insulator (SOI) technology, the flatness issue is mostly ameliorated (e.g. [5]-[7]). The biggest remaining obstacle in SOI MEMS is the inherent lack of out-of-plane motion. A variety of optical applications in telecommunications, as well as in bio-medicine require new degrees of freedom of out-of-plane motion, in addition to the traditional SOI-MEMS in-plane x-y displacement, are necessary. Traditionally, SOI-MEMS actuators have provided only in-wafer-plane motion. For optical applications such as scanning micromirrors, a variety of methodologies are investigated to provide the needed additional degrees of freedom (DoF). Particularly of interest is providing 1DoF (or single-axis) and 2DoF (two-axis) rotation of micromirrors. There is also demand for micromirrors with independently controlled rotation and pistoning motion [4].

Of interest was to enable fabrication of vertically displaced structures to provide conversion of in-plane actuation to out-of-plane actuation and rotation, or to enable fabrication of vertical combdrives and directly convert electrostatic force to rotation. Vertically staggered silicon-on-insulator (SOI) combdrives perform well for single-sided rotation applications [5],[6] and demonstrate advantages of SOI-MEMS with respect to surface-micromachined examples of vertical combdrives [4]. Recently, the SOI process was improved to provide self-alignment of upper and lower combfingers [10]. However, in these previous processes, no isolation is available between combdrive fingers in either upper or lower combdrives, limiting devices to one-sided rotation. Rotation of devices is accompanied by undesired downward and lateral actuation due to the electrostatic force which is undesirable for phased-array applications. Also, the support beams are full thickness SOI device layer beams which are stiff for torsion-rotation and especially inadequate for pistoning actuation. Lastly, the upper and lower comb-finger sets are separated by the thickness of insulating oxide (~ 1 μm), requiring large biasing (pre-tilting) of devices before the comb-fingers are adequately engaged. Pre-engagement of vertical comb-fingers is highly desirable for well-behaved performance at lower

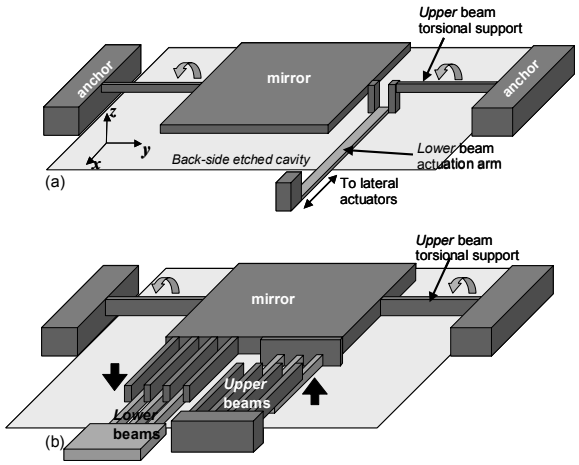

Figure 1. Schematic of the applications of the multi-level beams concept implemented in SOI device layer: (a) vertically displaced beams are used to convert lateral motion to rotation (b) vertically displaced beams in the device layer directly produce vertical actuation and rotation from electrostatic force.

demonstrated in a silicon optical scanner fabricated by eutectic bonding assembly [11]. The latter process suffers from difficult alignment between comb-fingers and utilizes metals and alloys that can reduce repeatability and reliability of device operation. The fabrication process presented in this work is a 4-mask SOI process that alleviates the above limitations. Namely: 1) all combfingers are fabricated in the device layer allowing isolated independently powered vertical combdrive sets. This enables independent up- or down- pistoning and bi-directional rotation; 2) comb-fingers are timed etched such that there is several microns of pre-engagement (overlap); 3) support beams can be of any desired thickness for lower-voltage operation, and optimized rotation vs. vertical pistoning compliance; 4) masks for etching of comb-fingers are self-aligned by a single mask; 5) structures are made in monolithic single-crystal silicon for repeatable and reliable operation.

Providing the capability for conversion of in-plane actuation to vertical actuation and/or rotation would enable a variety of high-performance micro-optical elements. Achieving that goal requires that the SOI-MEMS include structures that are vertically displaced from each other. If such vertically displaced single-crystal silicon (SCS) beams were available, there would be two possibilities for achieving vertical actuation and/or rotation: a) conversion of motion from adjacent lateral actuators to torque rotation by utilization of their vertically displaced sheer centers, as first proposed in [7], or b) direct vertical actuation, i.e. electrostatically, or thermally. These are illustrated in Fig. 1.

In the example of Fig. 1a, a micromirror and its torsional support beams that allow micromirror rotation are vertically displaced above the actuation arm. Therefore if the actuation arm is laterally (in-plane) pushed or pulled by any adjacent lateral actuator, torque is applied on the support beams, which rotates the mirror structure, a concept introduced in [7]. Because the beams are micromachined at different vertical levels, they are termed *Lower* and *Upper* beams (Fig. 1a).

In Fig. 1b on the other hand, *Lower* and *Upper* silicon beams are placed closely and interleaved to create vertical combdrive

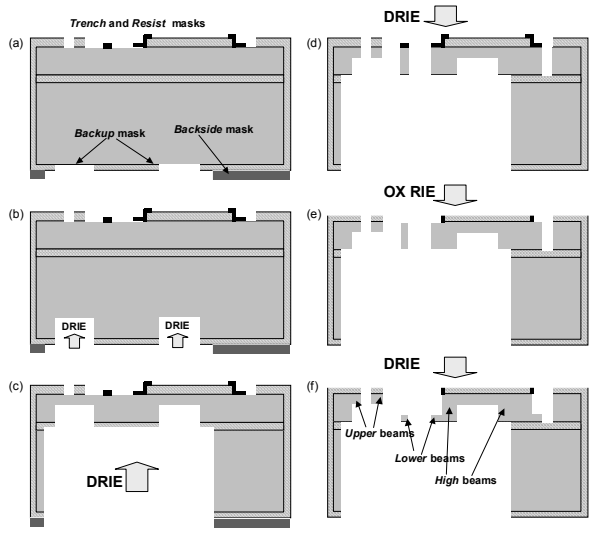

Figure 2. Schematic etching process steps for first version of the process in Sec. IIA.

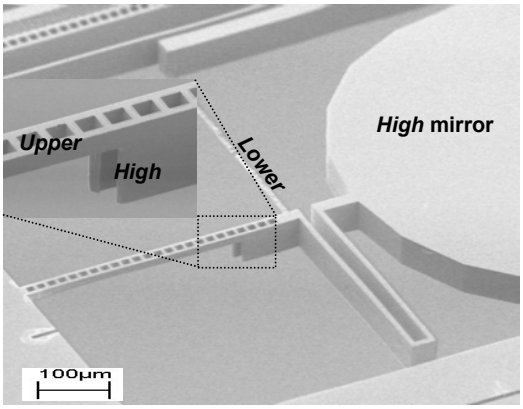

Figure 3. SEM images of a scanning micromirror [8] fabricated as described in Section IIa. Beams at three different levels are fabricated, Lower*,* Upper*, and* High*. Micromirror achieved 20° of optical deflection when combdrive pulls the Lower beam achieving torque around the perforated* Upper *support beam.*

structure, which converts electrostatic force directly to rotation, as previously demonstrated in [5]. However, unlike in previous work, the concept in Fig. 1b implies monolithic fabrication out of a single slab of single-crystal silicon (SCS) with several advantages: comb-fingers are pre-engaged giving significantly better performance at lower voltages [3], combdrives can be oriented to actuate *Up* or *Down* as illustrated in Fig. 1b, no bonding processes affect the actual device which itself is fully monolithically fabricated, and easier access to all the electrodes in a given device from the top side, also readily integrated with silicon integrated circuits. Finally, unlike in previous processes, the comb-finger etch-masks are self-aligned to the same mask, as will be explained in detail in Sec. IIB(ii).

To achieve the above structures we need the capability of etching a monolithic slab of Si to different depths from the front- and back-side. The process requires selective, multilevel etching [12] of SOI wafers, using deep reactive ion etching (DRIE) [13],[14]. The timed etch from front and back of device layer results in the various types of beams.

II. FABRICATION PROCESS

Two distinct versions of the process have been developed and demonstrated. The first version of the process has the advantage that it can be applied on any SOI wafer, i.e. it does not require actual SOI wafer preparation which includes a silicon fusion bonding step. The second version of the process includes necessary SOI wafer preparation by bonding which may be a drawback, but there are many advantages - the most important of which is that it provides very accurate beam alignment for high performance vertical combdrive fabrication.

A. Multilevel-beam SOI-MEMS: Front- and back-side multilevel DRIE for 3-level beam SOI-MEMS

The process requires four photolithography masks – three for the desired 3-level beams, and one for the bulk backside etch. The latter, *Backside* mask provides dry release for devices in the SOI device layer, as well as space for rotation and vertical displacement of structures. Also, in this process it has an additional role. It is used to provide access to the backside of the SOI device layer during the fabrication process itself, so that the *Backup* mask can be applied from beneath the device layer giving as a result the *Upper* beam of Fig. 1.

i) SOI Wafer Preparation

The fabrication process begins with bonded and double-side polished 100 mm diameter SOI wafers with desired device layer thickness (in this work 50 μm), with a 2 μm insulating oxide layer, and with a 300 μm thick silicon handle wafer. Each SOI wafer is either purchased or fabricated from two n-type doped prime-quality silicon wafers as follows. One wafer, intended for the SOI handle is purchased double-side-polished with accurate thickness of 300±1 μm. The second wafer which is to become the device layer in the SOI wafer is n-type prime wafer, standard thickness 525±25 μm, and single-side polished. A wet thermal oxide of 1 μm is grown on both wafers. Both wafers are then cleaned for 600 s in the *piranha* bath (2 l of H_2SO_4 + and 100 ml of H_2O_2) heated at 120°C, followed by de-ionized water rinsing and spin-drying. Immediately after spin-drying, the wafers' polished sides are put in contact, causing fusion pre-bonding of oxide surfaces. This is followed by an anneal with N_2 flow of 1

hour at 1100°C. Such wafers are then sent for grinding and polishing back from the thicker, device wafer's side, down to the total SOI wafer thickness of 353 μm (for 50 μm device-layer thickness.)

ii) Preparation of masks

The wafer first undergoes a 1.5 μm wet thermal oxidation. First mask *(Trench)* for deep front-side trenches is then etched into the oxide on the front side of the wafer, stopping on silicon. Then, 0.75 μm of low-temperature oxide (LTO) is deposited on the wafer to prepare the second front-side mask. Second mask *(Resist)* for protection of shallow front-side etches is etched into the LTO, again stopping on silicon in some areas, and stopping on the thermal oxide in other areas. Both masks are now transferred onto oxide layers on the wafer for later etching, and the front side of the wafer is thus ready for DRIE. This can be seen on the top surface schematic in Fig. 2a.

On the backside of the wafer, two masks are also employed. First mask defines so called *Backup* areas, i.e. areas where device single crystal silicon (SCS) will be thinned from beneath achieving a thin, *Upper* beam of Fig. 1. This mask is etched into the thermal oxide on the backside, also depicted in schematic in Fig. 2a. Then, fourth mask (*Backside*) is applied with thick resist, usually ~8 μm thick G-line resist which will provide a good mask for the long back-side DRIE, as well as oxide RIE steps. At this point the wafer is fully prepared for the many etch steps.

iii) Backside DRIE

Backside etch process consists of multiple etches, as illustrated in Fig. 2b-c. First etch is timed, to a depth of about 80μm (Fig. 2b.) Then plasma oxide etch removes the *Backup* oxide mask, such that only areas with the *Backside* mask remain protected. Second DRIE is done until the deeper trench (areas already etched to 80 μm by *Backup* mask) reaches the insulating oxide. At the point when those areas exposed by *Backup* mask have reached the oxide on the entire wafer, the rest of backside area has about 60 μm of silicon

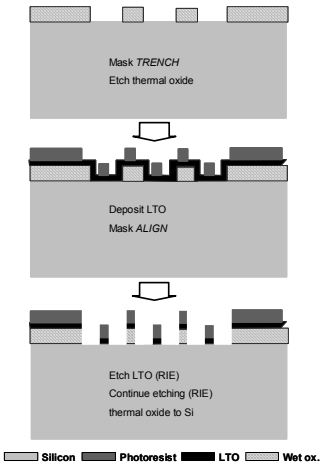

Figure 4. Mask self-alignment methodology: (a) since top side multilevel etching requires oxide masks of 2 different thicknesses [7], those masks are self-aligned by growing the first mask by 2 μm, and then cutting it back with the 2nd mask.

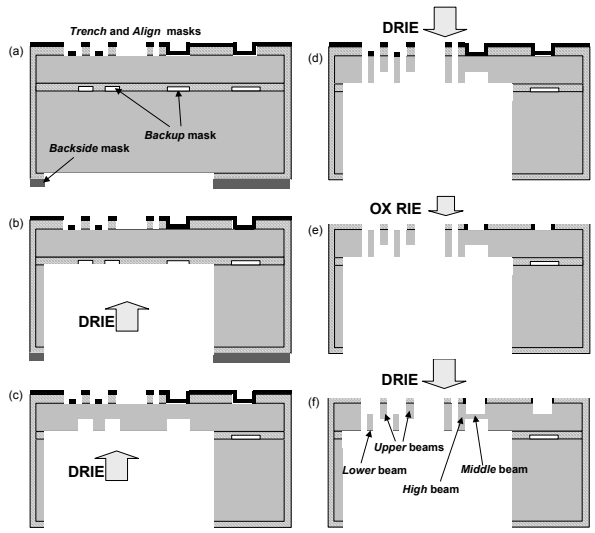

Figure 5. Schematic etching process steps for advanced version of the process in Sec. IIB.

remaining. Now the *Backup* mask, originally applied to the backside of the wafer, can be transferred onto the insulating oxide to be used to undercut the SOI device layer for *Upper* beams. The insulating oxide is thinned from 2.0 μm to 0.8 μm in those areas by oxide RIE. Then the remaining backside DRIE is done until all backside trenches reach the oxide, and clear the corners on the entire wafer which can require significant DRIE overetch. The wafer now goes back oxide RIE which is timed such that the thinner oxide (initially ~0.8 μm) is fully etched up to the SOI device layer silicon, while other areas have about 1.0 μm remaining. Effectively, the mask, *Backup* has been transferred from the backside surface onto the insulating oxide. The final backside step shown in Fig. 2c is to perform the actual *Backup* DRIE into the device layer. This etch is timed to leave a desired thickness of *Upper* beams which can vary from run to run depending on designs, etc. In most cases we etched about 35 μm of device layer silicon such that the *Upper* beam thickness would be ~15 μm. Lastly, the insulating oxide is fully removed by oxide RIE etch from the back-side.

iv) Front-side DRIE

First DRIE step etches through the device layer (Fig. 2d). Then, oxide plasma etch on the front side thins down oxide everywhere such that the *Resist* mask is fully removed, only *Trench* mask remains with ~0.7 μm thickness of wet thermal oxide (Fig. 2e). At this point, the *High* and *Upper* beams are complete. The second and final DRIE is done until the *Lower* beams are lowered to desired height, e.g. 8 μm. The final result is shown in the schematic in Fig. 2f.

Because our designed layout positions backside etches under *all* moving structures, those structures are inherently dry-released in the process due to the earlier backside etch and insulating oxide removal. Therefore, the wafer at this point contains fully functional MEMS ready for testing. This alleviates many issues with wet releasing of structures. Mechanical and electrical tests can be performed immediately after the DRIE step. In many cases, after initial testing, DRIE was continued to further lower the *Lower* beam, since the masks had not yet been removed.

v) Results

The above fabrication process was developed and utilized to fabricate laterally actuated micromirror devices [7]. To achieve the best performance, those devices require thin *Upper* and *Lower* beams, such that the micromirror torsional supports as well as the actuation arms are highly compliant. Because the beams are thin, their sheer centers are vertically separated by ~ 35-40 μm, which provides a significant torque distance for the lateral actuation concept [7]. Example of that structure is shown in Fig. 3. The micromirror is 12.5 μm thick, and 600 μm in diameter. The thinning from the original 50 μm thickness results in approximately two-fold increase in the resonant frequency for the micromirror, while the device still maintains flatness with radius-of-curvature (RoC) >4m [8]. The micromirror device uses the multi-level beam in the following manner – namely, the *Upper* beam is utilized as the torsional support while the *Lower* beam is the actuating arm. This micromirror demonstrated >20° of static, and >90° of dynamic optical beam deflection [8].

Since our process methodology employs timed DRIE to define thicknesses of beams critical to mechanical design, we monitored the thickness variations when possible. We have found that the thickness of a certain *Upper* beam design varied across the wafer by approximately ± 1.8 μm. This is a direct, and predicted result due to ~5% variation in etch rate over the 100 mm wafer for our DRIE recipes. The result for *Lower* beams was similar, with variation of approximately ± 2.0 μm.

B. Advanced multilevel-beam SOI-MEMS: 4-level beams and self-aligned vertical combdrive actuators

The process in Sec. IIA is adequate for many applications. However, because it utilizes front-to-back alignment to produce the beams it is not possible to align those structures with enough accuracy for implementation of high-performance vertical combdrives. To accomplish such accurate alignment and to allow the *Upper* beams to be of any feature size as available by stepper aligner available in this work, the process in Sec. IIA was improved to pre-embed the *Backup* mask into the insulation oxide while making the SOI wafer by bonding.

i) SOI Wafer Preparation

The preparation of the SOI wafer in this section is similar to that in the previous version of the process in Sec. IIA(i). The significant difference which provides the many advantages to this version of the process is that the oxide on the handle wafer's side intended for bonding is patterned before the bonding. Namely, after thermal oxide of 1 μm was grown on both wafers, the wafer intended for SOI handle is patterned with mask *Backup* and the oxide is etched down to silicon. After removing the mask and thorough cleaning of both wafers as described previously in Sec. IIA(i,) wafers are pre-bonded, annealed, and sent for grinding and polishing to desired device layer thickness.

ii) Mask preparation and self-alignment methodology

The two front-side masks are prepared utilizing oxides of two thicknesses, as in Sec. IIA(ii.) However, the mask preparation in this section is modified from Sec. IIA(ii) to

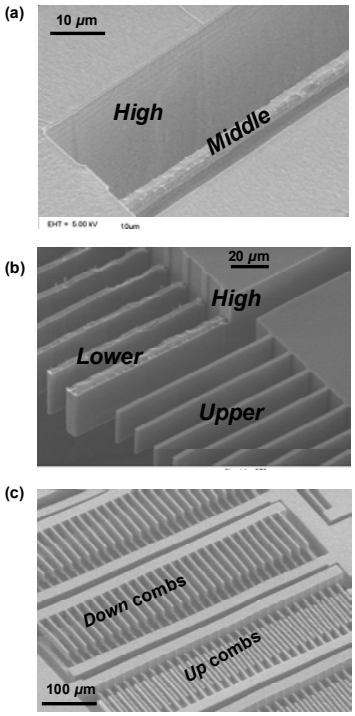

Figure 6. SEM of resulting structures after complete fabrication described in Sec. IIB: (a) Middle beam, fabricated by timed back- and front-side DRIE, and High beam structures around it; (b) test structure for Lower beam comb-fingers and Upper beam comb-fingers with comb-fingers separated; (c) actual fabricated combdrives with self-aligned Upper and Lower beam comb-fingers. Two independent sets are shown here, attached to the same support beam for choice of downward or upward actuation.

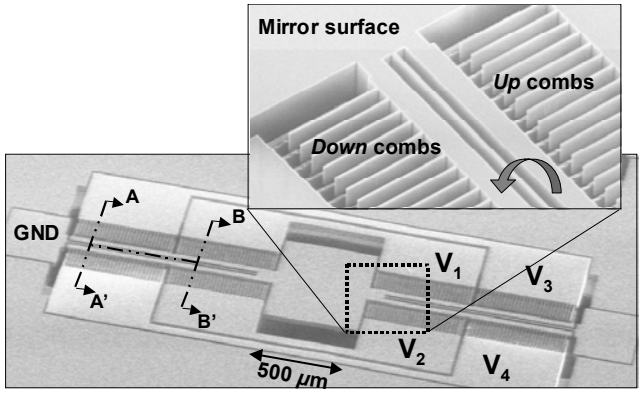

Figure 7. Application example: fabricated and characterized micromirror with 4 isolated vertical combdrive sets for up and down piston motion as well as bi-directional rotation [15].

provide self-alignment of both front-side masks for high-performance vertical combdrives. In addition, due to the fact that the *Backup* mask is already buried within the SOI wafer, the mask preparation process is different in that both of the front-side masks need to be aligned to that buried layer.

The SOI wafer, prepared as described in Sec. IIB(i) above, has 0.75 μm of thermal oxide grown on it. It is coated with photoresist and exposed in the wafer stepper with a blanket mask (no mask, clear reticle) in only two chip-locations, those used for stepper alignment (wafer edges), as done in previous work [5],[6]. This photoresist exposure and a subsequent front-side DRIE step down to the insulating oxide is used to recover the alignment mark features that were included in the *Backup* mask and were buried by the bonding process.

Front-side mask preparation with the following self-alignment methodology (depicted in Fig. 4) is then performed. The *Trench* mask patterns the thermal oxide on the top surface. But, to provide margin for subsequent self-alignment by the *Align* mask, the features of the *Trench* mask were previously enlarged from the designed features for the beams and other structures. Namely, the CAD layouts of *High* beam, *Upper* beams, and *Middle* beams are flattened, merged and grown by 2 μm on all sides to form the *Trench* mask. The thermal oxide is etched with this mask down to Si substrate, as in Fig. 4. It should be noted that this step does not require critical alignment since the buried *Backup* layer includes a ~2.0 μm margin for alignment since it is grown 2.0 μm larger than the desired final *Upper* beams.

Then, 0.75 μm of un-doped low-temperature oxide (LTO) is deposited on the wafer to prepare the second oxide front-side mask. Second mask, *Align* is applied as shown in Fig. 4. This mask contains the designs for *Lower* beams, as well as the designs for all other beams but this time with correct dimensions from the original layout. This step will therefore determine the final position of all structures and beams which will thereby be self-aligned to each other. As shown in Fig. 4, the mask is used to etch the LTO, and thermal oxide where-ever exposed. Both masks are now transferred onto oxide layers on the wafer for later etching, and the front side of the wafer is thus ready for DRIE. The resulting comb-fingers have been fabricated with near perfect alignment.

On the backside of the wafer, a single mask is employed and aligned to the front-side features. This, fourth *Backside* mask is applied with thick resist as before in Sec. IIA(ii). Because the backside of the wafer also has 1.5 μm of oxide from front-side preparation, the oxide is etched to Si substrate, and the wafer is prepared for DRIE steps as shown in Fig. 5a.

iii) Backside DRIE

Backside etch process consists of multiple etches, as illustrated in Fig. 5a-c. First DRIE is done until the etched trench reaches the insulating oxide. This exposes the insulating oxide and the buried *Backup* mask (Fig. 5b.) The insulating oxide is then thinned (by timed oxide etch) ~1.2 μm which exposes the device silicon layer in areas of buried *Backup* mask. The final backside DRIE step shown is to perform the actual *Backup* DRIE into the device layer. This etch is timed to leave a desired thickness of *Upper* beams which can vary from run to run depending on designs, etc. In most cases we etched about 20 μm of device layer silicon such that the remaining *Upper* beam thickness would be ~30 μm. Lastly, the insulating oxide is fully removed by oxide RIE etch from the back-side (Fig. 5c.)

iv) Front-side DRIE

The front-side DRIE steps are almost identical to those in Sec. IIA(iv). The steps are shown in Fig. 5d-f to better understand the formation of vertical combdrives. First DRIE etches through the device layer as shown in Fig. 5d. Then, oxide plasma etch of ~0.8 μm on the front side thins down oxide everywhere removing the thinner oxide mask (Fig. 5e.) The second and final DRIE is done until the devices are done, i.e. until the *Lower* beams are lowered to desired height of 30 μm. The final result is shown in the schematic in Fig. 5f.

v) Results

Examples of fabricated structures and beams are shown in SEM micrographs of Fig. 6. Due to the 20 μm etch of the device layer from the backside and the 20 μm etch of the layer from the front-side, the resulting *Middle* beams have average thickness of ~10 μm. Such a beam is shown in Fig. 6a. Also, due to the ~5% etch rate variation across the wafer, the thicknesses of resulting *Middle* beams vary from 8 μm to 12 μm. It is visible in the SEM that the surface of the beam is not smooth like the device layer surface because it is defined by timed DRIE. The smoothness can be improved with further etch recipe development.

Figure 6b shows resulting *Upper* and *Lower* beams, which

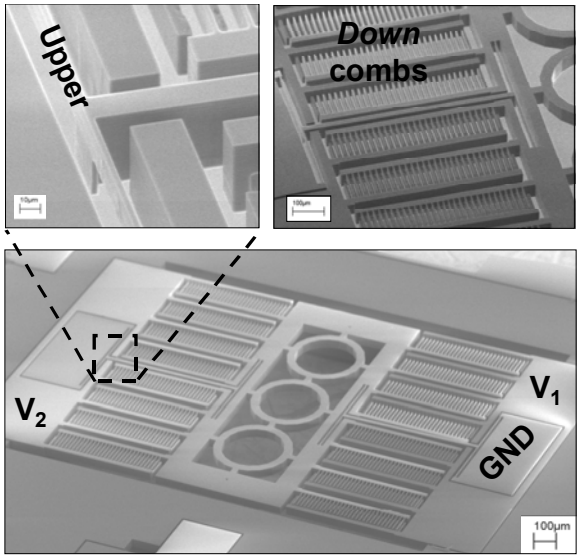

Figure 8. Application example: fabricated and characterized vertical actuator device for miniature 3D scanner applications with isolated vertical combdrive sets for low-voltage piston motion [16].

when interleaved as in Fig. 6c result in densely packed pre-engaged vertical combdrives. The SEM in Fig. 6c was taken after the electron beam was first used to charge one of the combdrive sets to result in full upward actuation. Therefore, the upward actuating combdrive is fully engaged (in position of maximum capacitance) while the combfingers of the downward actuating combdrive set is fully disengaged. Thus the main goal of fully isolated upward and downward actuating self-aligned combdrive sets was achieved.

III. APLICATION EXAMPES

In the first example [15] monolithic high aspect ratio Si micromirror device was demonstrated using the proposed fabrication methodology. As seen in Fig. 7, the device is suspended by torsional support beams and is structured to enable bi-directional single-axis rotation, as well as independent up- and down- pistoning actuation. Namely, due to the capability of employing isolated combdrive sets for upward or downward actuation, the device was designed to have four possible cross-sections for four modes of actuation. By electrically activating the proper pair of electrodes, the four actuation modes have been independently demonstrated [15]. Such a device with a 30 μm thick *Upper* support beam measured static optical beam deflection from –20° to 19° and bi-directional pistoning motion from –7.5 μm to 8.25 μm. In pistoning mode, the device exhibits resonance at 2619 Hz while in rotation mode at 1491 Hz. Another similar device which utilizes the highly compliant *Middle* beam (10 μm thick support beam) measured static optical beam deflection from –14° to 16° downward pistoning motion to –12.5 μm, all at <70 Vdc.

The second application example is a vertical actuator device for microlens actuation in 3D imaging applications [16] with emphasis on pure pistoning actuation and low-voltage operation. In the SEM micrographs of the device shown in Fig. 8, it can be seen that the device structure utilizes the self-aligned and pre-engaged *Upper* and *Lower* beams to form a large vertical combdrive. The suspension utilizes the *Upper* beam for compliant torsional operation which gives the low voltage of operation but also maintains good stability through the full range of actuation. Due to the availability of upward and downward pistoning, two types of devices were demonstrated. Single-directional devices (downward pistoning only) demonstrate maximum static downward displacement of 8 μm at 10 V_{DC}. Bi-directional devices demonstrate vertical actuation from -6.5 μm to +9 μm at max 12 V_{DC} and a vertical displacement of up to 55 μm peak-to-peak is achieved at the resonance near 400 Hz. At the full piston displacement of ~8 μm, the structure tilts very slightly by <0.034°, and compensation of that tilt using an isolated comb bank is demonstrated [16].

IV. CONCLUSIONS

The combination of back- and front-side multilevel etches with new alignment strategy allows for a new genre of high aspect ratio MEMS with additional degrees of freedom such as rotation and vertical actuation. One obvious application area as demonstrated is in MEMS micromirrors, micromirror arrays, phased-arrays, and other optical devices, as demonstrated by application examples to date.

The main limitation of the process is its dependence on the uniformity and precision of the timed DRIE steps, as some of those steps define thicknesses of structural beams. Our current focus is on improving the process yield, and achieving accurate control of layer thicknesses in the timed DRIE steps.

V. ACKNOWLEDGEMENT

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